D. Remarks

Claim 1 is believed to be distinguishable over the cited references. Claim 1 recites a memory cell having a first node, second node, transistor gate electrodes, and a capacitor having plates coupled between the first node and second node. A portion of one plate of the capacitor comprises a first interconnect wiring pattern. The first interconnect wiring pattern includes a plurality of conductive layers commonly etched into the same pattern with substantially aligned edges.

In contrast, U.S. Patent No. 5,780,910 (*Hashimoto et al.*) shows a capacitor element having a lower electrode and upper electrode that are separately etched into different patterns with edges that are not aligned with one another. FIG. 2(c) of *Hashimoto et al.* shows the pattern of the lower electrode (16). FIG. 2(d) of *Hashimoto et al.* shows the differently patterned upper electrode (19), which clearly has edges that are not aligned with those of the bottom electrode (16).

Because *Hashimoto et al.* teaches separate, non-aligned patterns for such electrodes, Applicant does not believe that the reference can be suggestive of claim 1.

U.S. Patent No. 6,104,053 (*Nagai*) teaches capacitors formed in a peripheral area, intentionally out of a memory cell area. Accordingly, *Nagai* is believed to teach away from connecting memory cell nodes to such plates, as recited in claim 1.

Claim 23 is also believed to be distinguishable from the cited references. Claim 23 recites a memory cell that includes a first data storage node, a second data storage node, a capacitor comprising a first plate coupled to the first data storage node, a second plate coupled to the second data storage node, and a third plate separated from the first and second plates by a capacitor dielectric. Also included is a plurality of wiring portions. Each wiring portion comprises a commonly patterned first conductive layer and dielectric layer. A first wiring portion forms the first plate and a second wiring portion forming the second plate. The dielectric layer forms the capacitor dielectric.

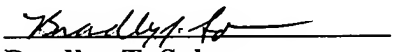
*Hashimoto et al.* shows an arrangement with but two capacitor electrodes, thus does not show and is not believed to suggest Applicant's three plate arrangement.

*Nagai* shows peripheral capacitors. However, the structure of *Nagai* does not show two portions, commonly patterned from a first conductive layer and a dielectric layer. Rather, *Nagai* shows two capacitors formed from different conductive/dielectric layers. See FIG. 1 of *Nagai* in which electrode 11 is separated from electrode 20 by layer 15, while electrode 20 is separated from electrode 40 by layer 22.

Claims 1, 5, 6, 22 and 23 have been amended.

Reconsideration of the patentability of these claims is respectfully requested.

Respectfully Submitted,



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